REMARKS

Claims 8-13, 15, and 17-26 are pending.

Claims 8, 11-13, 15, 17, 19, 23 and 24 were rejected under 35 U.S.C. 102(e).

Claims 8-15 and 17-22 were rejected under 35 U.S.C. 103(a).

Claim 16 is cancelled without prejudice.

Claims 8 and 20 have been amended.

Claims 25 and 26 are new.

No new matter is added.

Claims 8-13, 15, and 17-26 remain in the case for consideration.

Applicant requests reconsideration and allowance of the claims in light of the above amendments and following remarks.

Examiner Communication

Applicant thanks the Examiner for his time and suggestions, via his email on May 23, 2006, regarding claim language that may overcome the cited art.

Claim Rejections – 35 U.S.C. § 102

Claims 8, 11-13, 15, 17, 19, 23 and 24 were rejected under 35 U.S.C. 102(e) as being anticipated by Weis U.S. Patent Application Publication No. 2002/0196651 ("Weis").

Applicant respectfully traverses the rejection.

Claim 8 has been amended to recite *simultaneously* patterning the capping layer and the gate conductive layer as suggested by the Examiner. Support can be found in the Specification on page 5, lines 26-27, and FIG. 6, for example.

Weis teaches a much different method of forming a gate structure.

The Examiner acknowledges that Weis fails to teach *simultaneously* patterning the gate conductive layer (34, 40, and 42) and the capping layer 44. For example, Weis, on pages 4 and 5, beginning at paragraph [0029], teaches "After gate oxide 36 has been formed, gate polysilicon 34 is deposited within the deep trench, polished by CMP and recessed. Preferably, the deep trench is overfilled with gate polysilicon followed by a chemical mechanical polish (CMP) to the top of nitride layer 52 or to TTO layer 56. The polysilicon is then etched to approximately 70 nm below

the surface of the bulk silicon surrounding deep trench 20." Weis continues with several other process steps *before,* in paragraph [0036], a nitride cap 44 is *then* formed over a conductive stack.

Thus, Weis' approach is very different from simultaneously patterning a gate conductive layer and a capping layer, as required by claim 8.

Also to be considered, claim 8 requires forming a gate electrode having a first portion which rises over the semiconductor substrate and a second portion filling the trench by *simultaneously patterning the capping layer and the gate conductive layer*. In other words, simultaneously patterning the capping layer and the gate conductive layer results in the formation of the gate electrode. FIGS. 5 and 6 of the Specification illustrate this process. Weis, on the other hand, forms the gate conductive layer 34 with a recess (page 4, paragraph [0029]) in a separate step before forming the capping layer 44 (page 5, paragraph [0036]) on an already-formed conductor stack.

Thus, when comparing the limitations of claim 8 with the method taught by Weis, one can readily see that Weis fails to anticipate each and every limitation of this claim.

Claims 11, 14, 15, 17, and 19 depend upon claim 8, and inherently include all of the limitations of the base claim. As discussed above, the prior art does not teach the limitations of the base claim much less the further embodiments of the dependent claims. Therefore, claims 11, 14, 15, 17, and 19 are allowable for their dependency and their own merits. Allowance of these claims is requested.

Claim Rejections – 35 U.S.C. § 103

Claims 20 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weis in view of Cha Korean Publication No. 2001-64328 ("Cha").

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Weis in view of Ishikawa et al U.S. Patent No. 6,482,701 ("Ishikawa").

Claims 8, 11, 14, 15, 17, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lu U.S. Patent No. 5,362,665 ("Lu") in view of Cha.

Claims 9, 10, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable Lu and Cha as applied to claims 8, 11, 15, and 19 above, and further in view of Ishikawa.

Claims 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lu and Cha as applied to claims 8, 11, 15, and 19 above, and further in view of Durcan et al U.S. Patent No. 6,780,732 ("Durcan").

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lu and Cha as applied to claims 8, 11, 15, and 19 above, and further in view of Chang et al U.S. Patent No. 6,509,233 ("Chang").

Applicant respectfully traverses the rejection.

Claim 20 recites a limitation substantially similar to that in claim 14, and amended claim 8. Thus, the arguments presented above apply as well to claim 20. Thus Cha fails to show or teach all of the limitations of claim 20. Combining Weis with Cha also fails to obviate the limitations of claim 20.

Claims 9-19 and 21-24 depend upon claims 8 and 20, respectively, and inherently include all of the limitations of their base claims. As discussed above, the prior art does not teach the limitations of the base claim much less the further embodiments of the dependent claims. Therefore, claims 9-19 and 21-24 are allowable for their dependency and their own merits. Allowance of these claims is requested.

New Claims

Claim 8 is rewritten as new claim 25 with additional limitations, particularly those of claim 14. Support can also be found in the Specification on page 5, lines 26-27, and FIG. 6, for example.

Claim 25 recites that forming the gate electrode comprises *recessing* the gate conductive layer that fills the trench to a depth of 500Å or less from the surface of the semiconductor substrate. Therefore, these processing steps to form a gate electrode in accordance with the claimed invention are quite different from the processing steps, explained above, to form a gate electrode as taught by Weis.

Applicant also respectfully submits that Cha cannot be combined with Lu to reject claim 9, of which limitations are included in claim 25. Cha teaches only a trench formed by an *isotropic* etch process, as evidenced by the rounded trench structure 22 in FIG. 1a. Lu, on the other hand, teaches an anisotropic etching to form the, apparently *rectangular*, holes 14, as in FIG. 3A. Thus, one skilled in the art would not combine Lu and Cha to arrive at the claimed

invention. In particular, claim 25 recites (a limitation from claim 9) forming a trench in the semiconductor substrate by forming a rectangular trench using an etch process. One skilled in the art would use anisotropic etching to form a rectangular trench, as claim 25 requires. Thus Cha fails to teach this limitation. For at least these reasons, applicant submits that claim 25, which includes the limitations of claims 9 and 14, is allowable because the rejections of claims 9 and 14 are based on an improper combination of Cha and Lu.

Also, claim 25 recites simultaneously patterning the capping layer and the gate conductive layer. As explained above regarding claim 8, the cited art fails to anticipate this limitation.

Claim 26 recites forming the capping layer immediately after forming the gate conductive layer. Support for this claim can be found in the Specification on page 5, lines 21-22, and FIG. 5, for example.

Conclusion

For the foregoing reasons, reconsideration and allowance of claims 8-13, 15, and 17-25 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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